

Application No.: 09/496,516  
Amendment dated: December 29, 2003  
Reply to Office Action of: September 30, 2003

SAR-12165A

**Remarks/Arguments:**

The drawings were objected to under 37 C.F.R. § 1.83 as not showing every feature of the invention specified in the claims. This ground for objection is overcome by the amended drawing of Fig. 9, submitted herewith. As required in the Office Action, Fig. 9 has been amended to include the receiving means, the data means and the signal generating means in the integrator and to include the receiving means and the clock synchronization means in the discriminator. Basis for this amendment may be found in claims 15 and 19 and at page 16, line 21 through page 19, line 15. With these amendments, drawing Fig. 9 is no longer subject to objection.

Claims 15-18 were rejected under 35 U.S.C. § 102(b) as being anticipated by Giles et al. This ground for rejection is respectfully traversed. In particular, Giles does not disclose or suggest "counter means for increasing a count value when the first signal includes the first data value and decreasing the count value when the first signal includes the second data value," as required by claim 15.

Whether the counter 18 in Giles et al. counts up or down is determined by the signals  $CS$  and  $\overline{CS}$ , the output signals of the exclusive OR gate 14 and the inverter 15. The input signals to the exclusive OR gate 14 are the received signal LS1 and a delayed version of this signal, LS2. Thus, the counter in Giles et al. is configured to count down when LS1 and LS2 are not equal and to count up when they are equal. (See column 3, line 61 through column 4, line 29). This does not meet the limitations of claim 15, however, because that claim requires the counter means to increase the count value when the first signal includes the first data value and to decrease the count value when the first signal includes the second data value. As described in the above-referenced passage, Giles et al. do not care about the value of the input signal but about the difference between the delayed and undelayed values. Consequently, Giles et al. does not meet the limitations of claim 15 and, so, claim 15 is not subject to rejection under 35 U.S.C. § 102(b) in view of Giles et al.

Claims 16-18 depend from claim 15 and are not subject to rejection under 35 U.S.C. § 102(b) in view of Giles et al. for at least the same reasons as claim 15.

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Applicants gratefully acknowledge that claims 19-24 are allowed.

The prior art cited but not applied has been considered but does not affect the patentability of any claim.

In view of the foregoing amendments and remarks, Applicants request that the Examiner reconsider and withdraw the objection to drawing Fig. 9 and the rejection of claims 15-18.

Respectfully submitted,



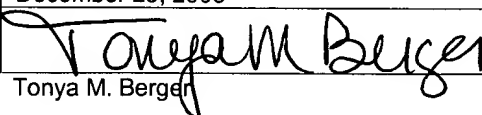
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Enclosure: Figure 9 (1 sheet)

Dated: December 29, 2003

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